aP4890K --- 1.4 Watt Audio Power Amplifier

FEATURES :

- 2.5V~5.5V Power supply.
- Thermal shutdown Protection.
- Low current shutdown mode
- No output capacitors and networks or bootstrap
- capacitors required
- Low noise during turn-on and turn-off transitions
- Shutdown pin high active.

GENERAL DESCRIPTION :

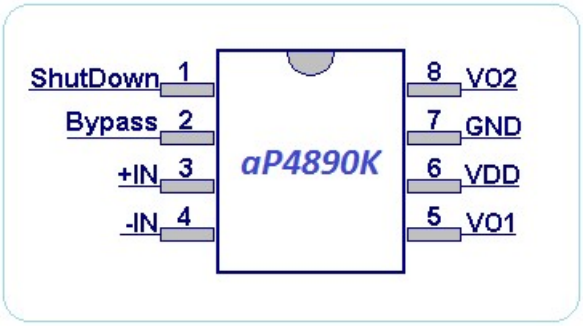
The AP4890K is a 1.4 Watt audio power amplifier. And the AP4890K primarily designed for high Quality application in other portable communication device.

It is capable of driving 8Ω speaker load at a continuous average output of 1.4W / 10% distortion (THD+N) from a 5.0V power supply. A feature of the AP4890K amplifier to switch BTL mode. And the AP4890K audio amplifier features low power consumption shutdown mode. It is achieved by driving the shutdown pin with logic high. Besides the AP4890K has an internal thermal shutdown protection feature.

The AP4890K amplifier was designed specifically to provide high quality output power with a minimal amount of external components. The AP4890K does not require output capacitors, and the AP4890K is ideally suited for other low voltage applications or portable electronic devices where minimal power consumption is a primary requirement.

APPLICATION :

- Portable electronic devices
- Mobile Phones
- PDAs



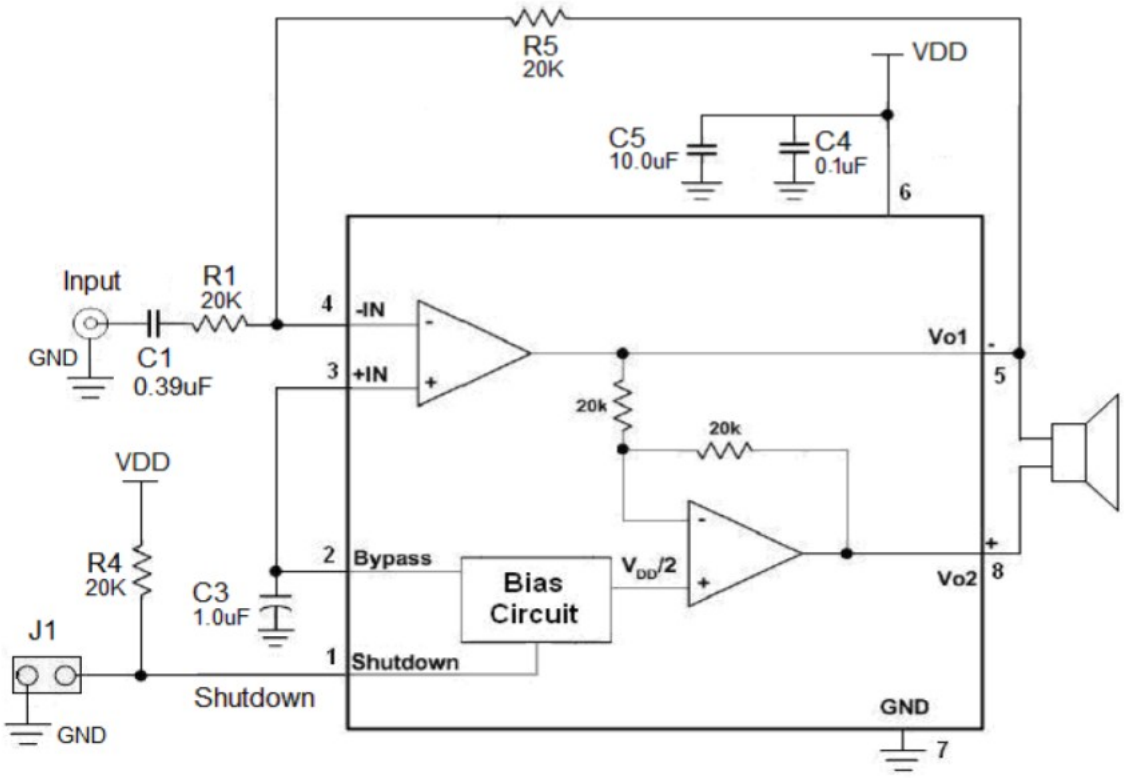
- **PIN DESCRIPTION :**

SYMBOL	Pin No	DESCRIPTION
SHUTDOWN	1	Shutdown the device. (when LOW level is shutdown mode)
BYPASS	2	Bypass pin
+IN	3	Positive Input
-IN	4	Negative Input
Vo1	5	Negative output
VDD	6	Power Supply
GND	7	Ground
Vo2	8	Positive Output

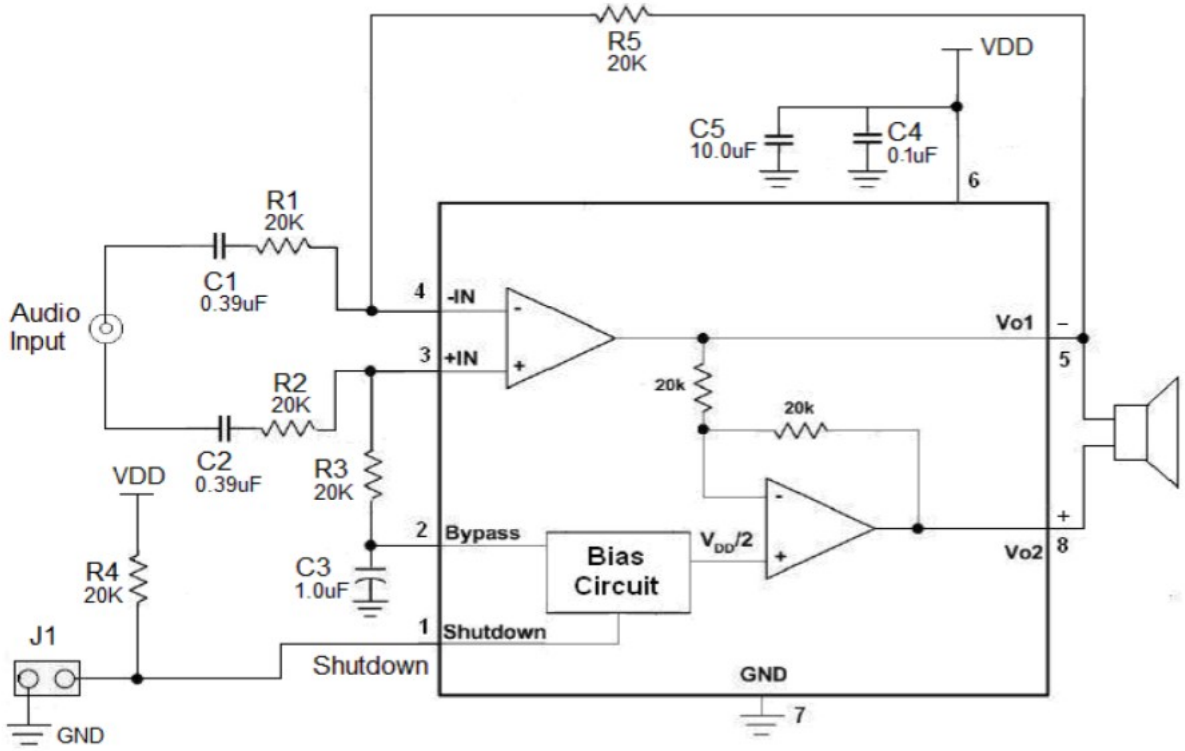
- **ABSOLUTE MAXIMUM RATINGS :**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6.0	V
Operating Temperature	T_A	-40 to 85(I grade)	℃
Input Voltage	V_I	-0.3V to VDD +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

- **APPLICATION CIRCUIT :**

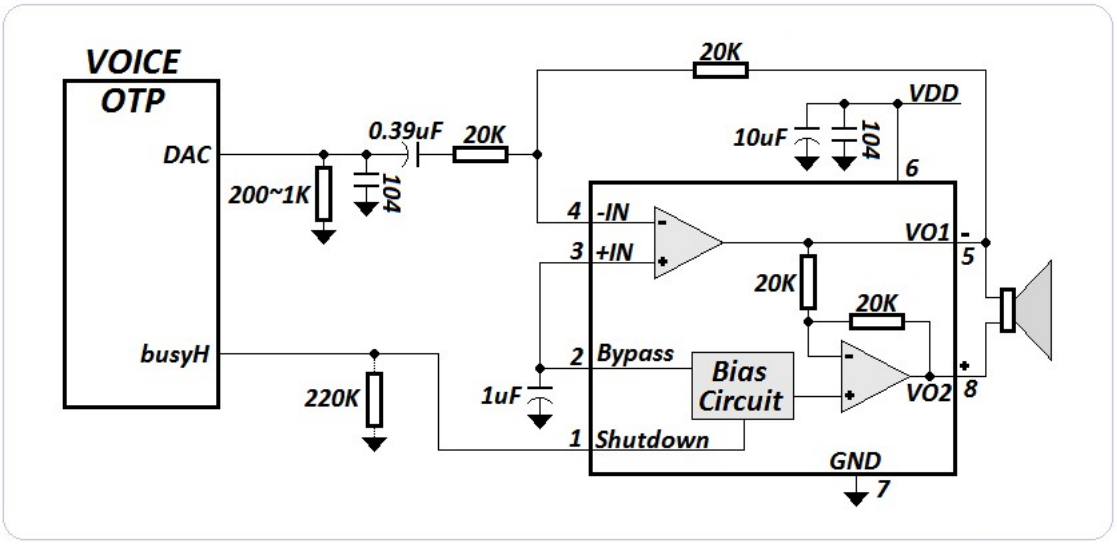


application schematic with single –ended input

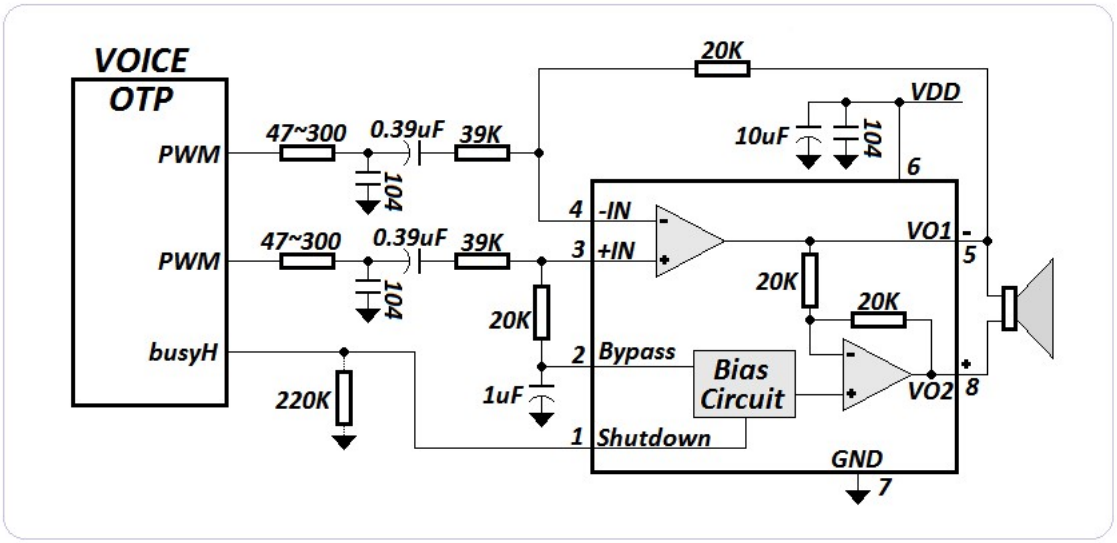


application schematic with differential input

- **VOICE OTP [DAC] + AP4890K APPLICATION :**



- **VOICE OTP [PWM] + AP4890K APPLICATION :**



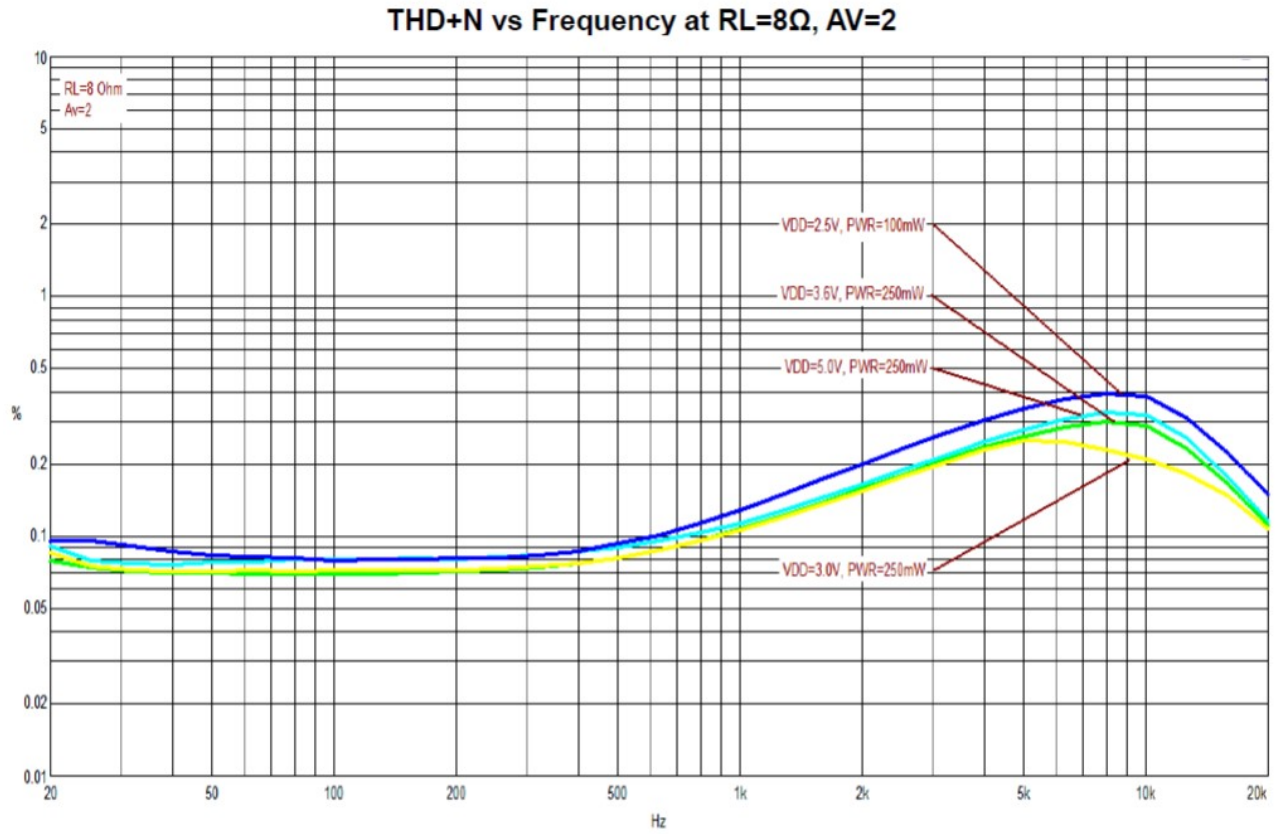
● DC ELECTRICAL CHARACTERISTICS (TA=25℃) :

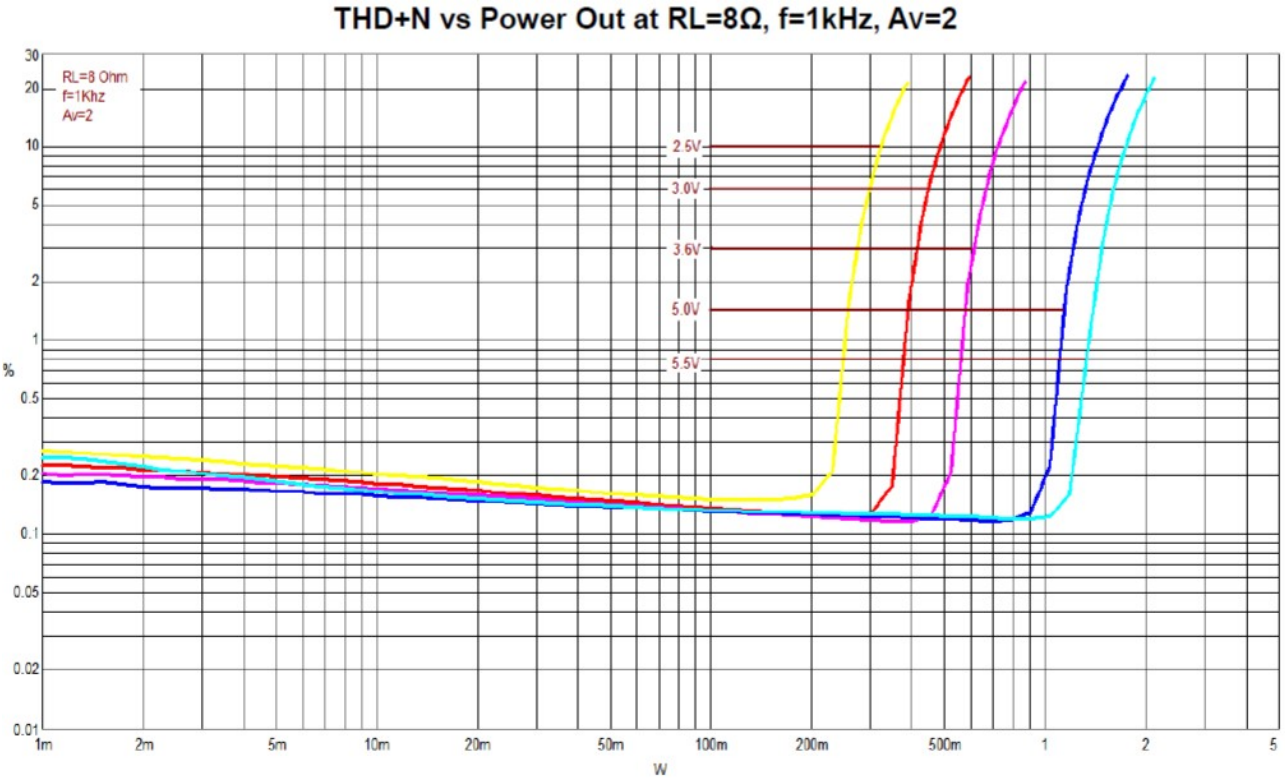
PARAMETER	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Power Supply Current	IDD	VIN = 0V, IO = 0A,8Ω Load	VDD =5V	-	6.0	18.0	mA
			VDD =3V	-	5.0	15.0	mA
Shutdown Current	ISD	VSHUTDOWN = VDD		-	0.1	2.0	μA
Output Offset Voltage	VOS			-	7.0	50.0	mV
Resistor Output to GND	ROUT-GND			-	9.5	-	kΩ
Output Power	Po	THD = 10%, f=1kHz,RL=8Ω	VDD =5V	-	1.4	-	W
		THD = 1%, f=1kHz ,RL=8Ω		-	1.1	-	
		THD = 10%, f=1kHz,RL=8Ω	VDD =3V	-	480	-	mW
		THD = 1%, f=1kHz,RL=8Ω		-	375	-	
Total Harmonic Distortion+ Noise	THD+N	Po=780 mWrms; f = 1kHz	VDD =5V	-	0.1	-	%
		Po=265 mWrms; f = 1kHz	VDD =3V	-	0.12	-	%
Power Supply Rejection Ratio	PSRR	Vripple= 200mV sine p-p, Input = Floating	VDD =5V	-	66 (Ps1)	-	dB
			VDD =3V	-	62 (Ps2)	-	dB
Wake-up time	TWU	Bypass Cap.=1.0uF	VDD =5V	-	145	-	Ms
			VDD =3V	-	82	-	ms
Thermal Shutdown Temperature	TSD			**150**	170	190	℃
Shut Down Time	TSDT	8 Ω load		-	1.0	-	ms

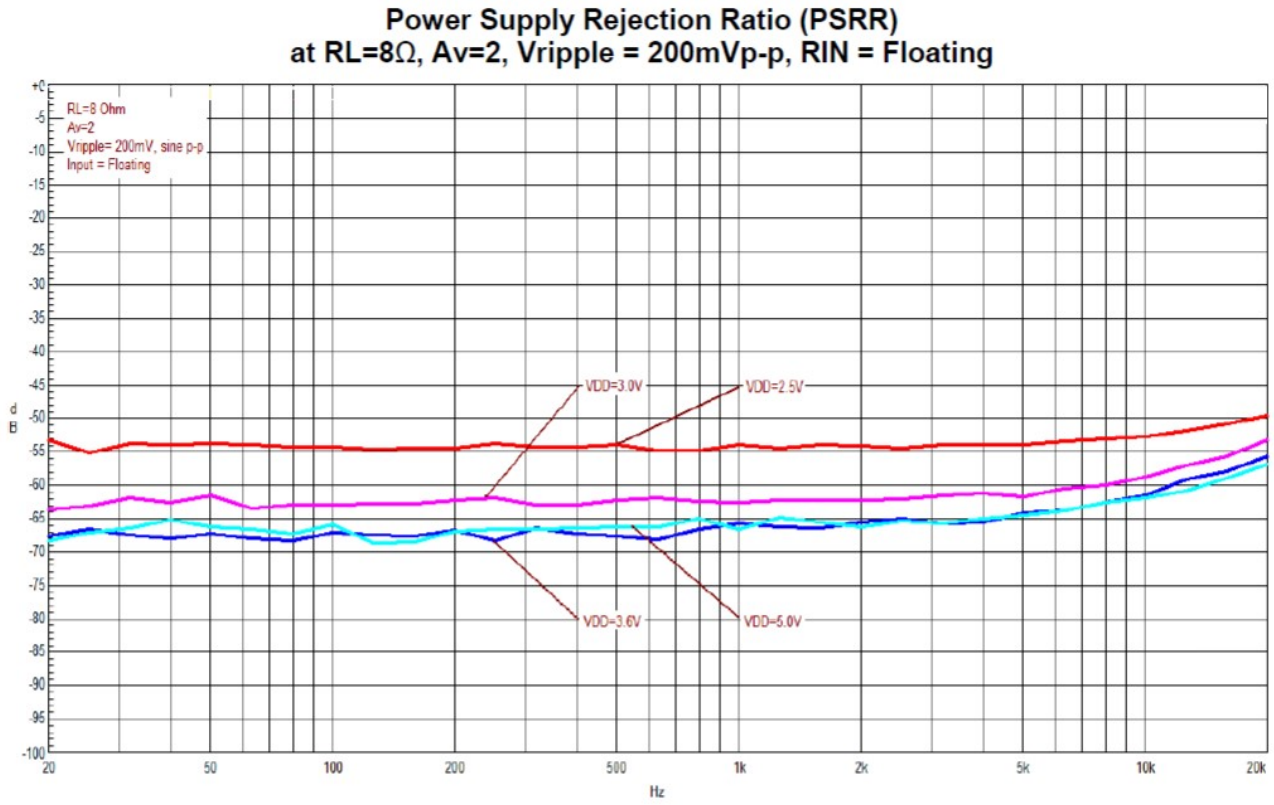
ps1 : 66 dB(217Hz) / 66 dB(1KHz)

ps2 : 62 dB(217Hz) / 62 dB(1KHz)

- **TYPICAL PERFORMANCE CHARACTERISTICS :**







● APPLICATION INFORMATION :

BRIDGED CONFIGURATION EXPLANATION

As shown in Figure 1, the AP4890K has two operational amplifiers internally, allowing for a few Different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to RIN while the second amplifier's gain is fixed by the two internal 20kΩ resistors.

Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

AVD= 2 X (Rf / RIN) ……(1)

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it Provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

A bridge configuration, such as the one used in the AP4890K, also creates a second advantage over Single -ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

● INPUT CAPACITORS (Ci) :

The AP4890K input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in equation Equation 2.

fc = (1/ 2πRiCi) ……(2)

Equation 3 is reconfigured to solve for the input coupling capacitance.

Ci = (1/ 2πRifc) ……(3)

For example

In the table 1 shows the external components. Rin in connect with Cin to create a high-pass filter.

Table 1. Typical Component Values

Reference	Description	Not
Ri	20KΩ	1% tolerance resistors
Ci	0.39uF	80%/–20%

Ci = 1 / (2πRifc)

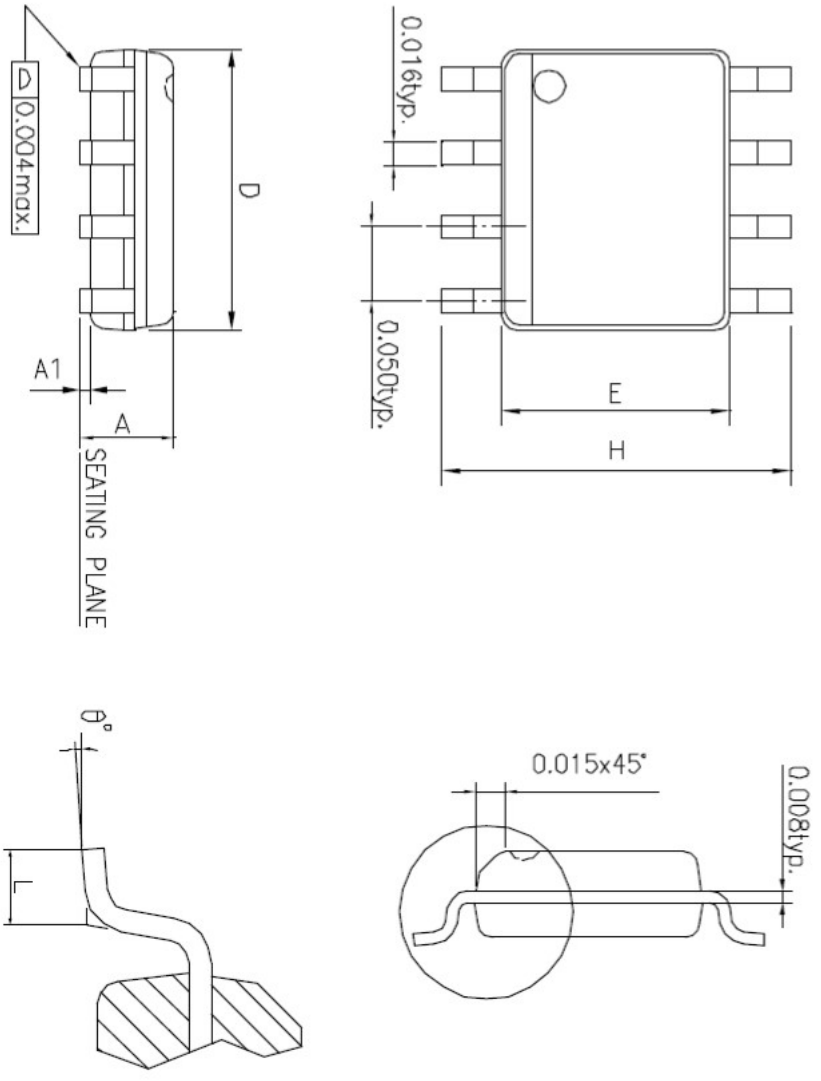
Ci = 1 / (2 π x 20KΩ x 20Hz) = 0.397uF …….. Use 0.39uF

● POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor location on both the bypass and power supply pins should be as close to the device as possible.

- **SOP8 : (150 mil)**

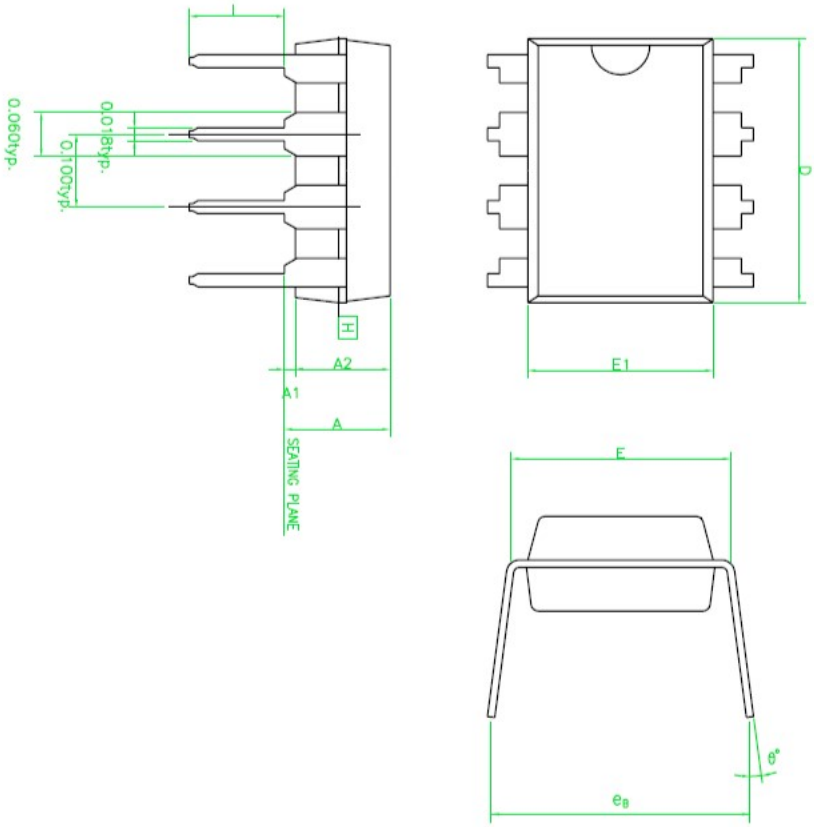


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AA
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

- **DIP8 : (300 mil)**



SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-001 BA
2."D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3.eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4.POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5.DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6.DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.